REMARKS

Claims 1-11 are pending in this application. By this Amendment, claim 1 has been amended. The applicant respectfully submits that no new matter has been added. It is believed that this Response is fully responsive to the Office Action dated September 10, 2002.

AS TO THE MERITS:

As to the merits of this case, the Examiner maintains the following rejections:

1) claims 1-5, 7, 8 and11 stand rejected under 35 U.S.C. §103(a) as being obvious over **Saito** (U.S. Patent No. 5,773,853) in view of Applicant's prior art Figs. 1 and 2;

2) claim 6 stands rejected under 35 U.S.C. §103(a) as being obvious over **Saito** in view of Applicant's prior art Figs. 1 and 2 and **Nakanishi** (U.S. Patent No. 5,477,066); and

3) claims 9 and 10 stand rejected under 35 U.S.C. §103(a) as being obvious over **Saito** in view of Applicant's prior art Figs. 1 and 2 in view of **Kuroda et al.** (U.S. Patent No. 5,837,565).

Each of these rejections are respectfully traversed.

In response to Applicant's argument that in **Saito** a peak of distribution of In will exist in an end portion of a surface side of the GaAs/InGaAs layer (25) since in col 7, lines 30 to 40 (Fig. 4B) of **Saito**, it is described that when $In_yGa_{1-y}As$ layer (23) and GaAs layer (24) is deposited with 20 cycles and a multi-layer made of GaAs/InGaAs layer (25) is formed, and "y" of $In_yGa_{1-y}As$ layer (23) becomes big as it becomes next deposition, the Examiner takes the following position:

> Applicant state that Saito discloses that a "peak of distribution of In will exist in an end portion of a surface side of GaAs/InGaAs layer (25) from the above description." However, it is not clear as to how Applicant came to the conclusion that In exist in the end portion based on column 7 lines 30-40. Applicant has not presented evidence that In will exist in the end. Therefore, the arguments as indicated above are not deemed persuasive.[1]

In the first office action, the phrase of "a graded channel layer" in claim 1 was amended such that "a graded channel layer formed on the substrate, and formed a second compound semiconductor layer of which an energy band gap is made narrower inside than both ends by making a peak of a distribution of one constituent element exist in the inside except the both ends in a thickness direction and dosed with an impurity".

Further, it was alleged that in Saito, a peak of distribution in In will exist in an end portion of a surface side of the GaAs/InGaAs layer (25) on the basis of the description (Col. 7, lines 30-40 (Fig. 4B)).

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[1]Please see, lines 14 - 20, page 6 of the outstanding Action.

By the way, it is respectfully noted that the GaAs/InGaAs layer (25) in Saito is a buffer layer, and not a channel layer (Col. 7, lines 29-30). Instead, the active layer 27 in Saito corresponds to the graded channel layer of claim 1.

The examiner indicates $In_yGa_{1-y}As$ layer (23) in Saito corresponds to the graded channel layer in claim 1, but $In_yGa_{1-y}As$ layer (23) in Saito is the layer which constitutes the above-mentioned buffer layer (GaAs/InGaAs layer (25)).

In claim 1 of the application, the peak of carrier density distribution is set to a position into the inside not the surface of the channel layer. Therefore, even if the fluctuation of the gate voltage, the reduction of the gate voltage, etc. is caused, the steep increase/decrease of the carrier density in the channel layer is suppressed and also the mutual conductance that is higher and more stable than the prior art is obtained.

In Saito, it is only described that having a composition of In of the buffer layer (GaAs/InGaAs layer (25)) changed in the inside of the layer, and is not described about a composition of In of channel layer. Also, it is not described in Saito that the above-mentioned purpose and advantage of claim 1.

Accordingly, it is unthinkable that persons skilled in the art set up the channel layer on the basis of Saito such that an energy band gap is made narrower inside than both ends by making a peak

of a distribution of one constituent element exist in the inside except the both ends in a thickness direction.

In view of the aforementioned remarks, claims 1 - 11 are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made to the by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, Applicants respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosures: Version with markings to show changes made

VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/893,477

IN THE CLAIMS:

Claim 1 has been amended to read as follows:

1. (Twice amended) A compound semiconductor device comprising:

a substrate formed of a first compound semiconductor;

a buffer layer formed on the substrate;

a graded channel layer formed on the buffer layer [substrate], and formed of a second compound semiconductor layer of which an energy band gap is made narrower inside than both ends by making a peak of distribution of one constituent element exist in the inside except the both ends in a thickness direction and doped with an impurity;

a barrier layer formed on the graded channel layer;

a gate electrode formed on the barrier layer to come into Schottky-contact with the barrier layer; and

a source electrode and a drain electrode formed on both sides of the gate electrode to flow a current into the graded channel layer via the barrier layer.